REMARKS

Applicants respectfully request reconsideration of the present U.S. patent application. Claims 1-22 stand rejected under 35 U.S.C. § 103. Claims 1 and 13 have been amended. Claim 3 has been canceled. No claims have been added. Therefore, claims 1, 2 and 4-22 remain pending.

Claim Rejections - 35 U.S.C. § 103

Rejections of Claims 1, 3, 4, 6-11, 13, 14, 16-18, 20 and 21 based on *Otani* and *Holt*

Claims 1, 3, 4, 6-11, 13, 14, 16-18, 20 and 21 were rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent Application US2001/0022534 filed by Otani (*Otani*) in view of Electronic Circuits – Digital and Analog by Holt (*Holt*). Claim 3 has been canceled. Therefore, the rejection of claim 3 under 35 U.S.C. § 103 is moot. For at least the reasons set forth below, Applicants submit that claims 1, 4, 6-11, 13, 14, 16-18, 20 and 21 are not rendered obvious by *Otani* in view of *Holt*.

Claim 1 recites the following:

> a node connecting an output of the impedance inverter circuit and an output of the second amplifier, the node configured to combine the first and second delayed output signals, thereby creating an amplified output signal; ...

Claim 13 is a method claim, and recites similar limitations.

Otani discloses a push-pull power amplifier that includes power amplifying elements and phase converters. See Fig. 2; Paragraph [0023]. A signal is input through a first terminal, distributed to an antiphase signal by means of a phase converter at the front end of the power amplifying elements, amplified by means of the power amplifying elements, synthesized by a phase converter at the rear end of the power amplifying elements, and output through a second terminal. See Paragraphs [0023], [0026] and

[0027]. *Otani* does not disclose a node connecting an output of an impedance inverter circuit and an output of a second amplifier, the node configured to combine a first and second delayed output signals, thereby creating an amplified output signal. Thus, *Otani* fails to disclose at least one limitation of claims 1 and 13.

Examiner cites *Holt* for the proposition that it would have been obvious "to have provided *Otani* with a bias arrangement(s) for the first and second amplifiers ... and to select the bias point to be that of linear operation." See Office Action, page 3. Examiner does not assert that *Holt* discloses a node connecting an output of an impedance inverter circuit and an output of a second amplifier, the node configured to combine a first and second delayed output signals, thereby creating an amplified output signal.

Applicants do not necessarily agree with the Examiner's characterization of *Holt*, and expressly reserve the right to address the Examiner's characterization of *Holt* in any future Office Actions. However, regardless of whether Examiner's characterization of *Holt* is correct, *Holt* fails to cure the deficiencies of *Otani* pointed out by Applicants. Thus, *Otani* in view of *Holt* fails to disclose at least one limitation of claims 1 and 13. Consequently, claims 1 and 13 are not rendered obvious by *Otani* in view of *Holt* for at least the reasons set forth above. Applicants therefore respectfully request that the Examiner withdraw the rejections of claims 1 and 13 under 35 U.S.C. § 103.

Claims 4 and 6-11 depend from claim 1. Claims 14, 16-18, 20 and 21 depend from claim 13. Because dependent claims include the limitations of the claims from which they depend, Applicants submit that claims 4, 6-11, 14, 16-18, 20 and 21 are not rendered obvious by *Otani* in view of *Holt* for at least the reasons set forth above.

Rejections of Claims 2 and 15 based on *Otani*, *Holt* and *Cheng*

Claims 2 and 15 were rejected under 35 U.S.C. § 103 as being unpatentable over *Otani* in view of *Holt*, and further in view of Cheng et al., U.S. Patent Application No. 2002/0190790 (*Cheng*). For at least the reasons set forth below, Applicants submit that claims 2 and 15 are not rendered obvious by *Otani* in view of *Holt* and *Cheng*.

As explained above, *Otani* in view of *Holt* fails to disclose a node connecting an output of an impedance inverter circuit and an output of a second amplifier, the node configured to combine a first and second delayed output signals, thereby creating an amplified output signal, as recited in claims 1 and 13. Examiner cites *Cheung* with regard to selectively supplying bias voltages. See Office Action, page 5. Examiner does not assert that *Cheng* discloses a node connecting an output of an impedance inverter circuit and an output of a second amplifier, the node configured to combine a first and second delayed output signals, thereby creating an amplified output signal.

Applicants do not necessarily agree with the Examiner's characterization of *Cheng*, and expressly reserve the right to address the Examiner's characterization of *Cheng* in any future Office Actions. However, regardless of whether Examiner's characterization of *Cheng* is correct, *Cheng* fails to cure the deficiencies of *Otani* in view of *Holt* pointed out by Applicants. Thus, *Otani* in view of *Holt* and *Cheng* fails to disclose at least one limitation of claims 1 and 13. Consequently, claims 1 and 13 are not rendered obvious by *Otani* in view of *Holt* and *Cheng* for at least the reasons set forth above.

Claim 2 depends from claim 1. Claim 15 depends from claim 13. Because dependent claims include the limitations of the claims from which they depend, Applicants submit that claims 2 and 15 are not rendered obvious by *Otani* in view of *Holt*

and *Cheng* for at least the reasons set forth above. Applicants therefore request that the Examiner withdraw the rejections of claims 2 and 15 under 35 U.S.C. § 103.

Rejections of Claims 5 and 19 based on *Otani*, *Holt* and *Sedra*

Claims 5 and 19 were rejected under 35 U.S.C. § 103 as being unpatentable over *Otani* in view of *Holt*, and further in view of *Sedra*. For at least the reasons set forth below, Applicants submit that claims 5 and 19 are not rendered obvious by *Otani* in view of *Holt* and *Sedra*.

As explained above, *Otani* in view of *Holt* fails to disclose a node connecting an output of an impedance inverter circuit and an output of a second amplifier, the node configured to combine a first and second delayed output signals, thereby creating an amplified output signal, as recited in claims 1 and 13. Examiner cites *Sedra* with regard to replacing single-stage amplifiers with multiple-stage amplifiers. See Office Action, pages 5-6. Examiner does not assert that *Sedra* discloses a node connecting an output of an impedance inverter circuit and an output of a second amplifier, the node configured to combine a first and second delayed output signals, thereby creating an amplified output signal.

Applicants do not necessarily agree with the Examiner's characterization of *Sedra*, and expressly reserve the right to address the Examiner's characterization of *Sedra* in any future Office Actions. However, regardless of whether Examiner's characterization of *Sedra* is correct, *Sedra* fails to cure the deficiencies of *Otani* in view of *Holt* pointed out by Applicants. Thus, *Otani* in view of *Holt* and *Sedra* fails to disclose at least one limitation of claims 1 and 13. Consequently, claims 1 and 13 are not

rendered obvious by *Otani* in view of *Holt* and *Sedra* for at least the reasons set forth above.

Claim 5 depends from claim 1. Claim 19 depends from claim 13. Because dependent claims include the limitations of the claims from which they depend, Applicants submit that claims 5 and 19 are not rendered obvious by *Otani* in view of *Holt* and *Sedra* for at least the reasons set forth above. Applicants therefore request that the Examiner withdraw the rejections of claims 5 and 19 under 35 U.S.C. § 103.

Rejections of Claims 12 and 22 based on *Otani*, *Holt* and *Taniguchi*

Claims 12 and 22 were rejected under 35 U.S.C. § 103 as being unpatentable over *Otani* in view of *Holt*, and further in view of U.S. Patent No. 5,162,756 issued to Taniguchi et al. (*Taniguchi*). For at least the reasons set forth below, Applicants submit that claims 12 and 22 are not rendered obvious by *Otani* in view of *Holt* and *Taniguchi*.

As explained above, *Otani* in view of *Holt* fails to disclose a node connecting an output of an impedance inverter circuit and an output of a second amplifier, the node configured to combine a first and second delayed output signals, thereby creating an amplified output signal, as recited in claims 1 and 13. Examiner cites *Taniguchi* with regard to replacing single-stage amplifiers with multiple-amplifier arrangements. See Office Action, pages 6-7. Examiner does not assert that *Taniguchi* discloses a node connecting an output of an impedance inverter circuit and an output of a second amplifier, the node configured to combine a first and second delayed output signals, thereby creating an amplified output signal.

Applicants do not necessarily agree with the Examiner's characterization of *Taniguchi*, and expressly reserve the right to address the Examiner's characterization of

Taniguchi in any future Office Actions. However, regardless of whether Examiner's characterization of *Tanaguchi* is correct, *Taniguchi* fails to cure the deficiencies of *Otani* in view of *Holt* pointed out by Applicants. Thus, *Otani* in view of *Holt* and *Taniguchi* fails to disclose at least one limitation of claims 1 and 13. Consequently, claims 1 and 13 are not rendered obvious by *Otani* in view of *Holt* and *Taniguchi* for at least the reasons set forth above.

Claim 12 depends from claim 1. Claim 22 depends from claim 13. Because dependent claims include the limitations of the claims from which they depend, Applicants submit that claims 12 and 22 are not rendered obvious by *Otani* in view of *Holt* and *Taniguchi* for at least the reasons set forth above. Applicants therefore request that the Examiner withdraw the rejections of claims 12 and 22 under 35 U.S.C. § 103.

CONCLUSION

For at least the foregoing reasons, Applicants submit that the rejections have been overcome. Therefore, claims 1, 2 and 4-22 are in condition for allowance and such action is respectfully solicited. The Examiner is respectfully requested to contact the undersigned by telephone if such contact would further the examination of the present application.

Respectfully submitted,

Dated: August 17, 2006

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